EN-OSFP800-2FR4

The 800G OSFP 2FR4 Transceiver is designed to transmit and receive serial optical data links up to 106.25 Gbps data rate (per channel) by PAM4 modulation format over single-mode fiber. It is a small-form-factor hot pluggable transceiver module integrated with high performance Sipho modulator. It is compliant with 800G Ethernet specs and OSFP MSA.

Features

- Hot-pluggable OSFP form factor
- 8 channels of 100G-PAM4 electrical and optical parallel lanes
- Dual Duplex LC optical interface
- Single +3.3V power supply
- Maximum link length of 2km on SMF fiber
- Power dissipation:<16W
- Operating temperature range: 0℃ ~ +70℃
- CMIS-compliant management interface with full module diagnostics and control through I^2C

Applications

- Data Centers
- Switch with 800G OSFP Port
- 800GBASE-2FR4 Ethernet & IB NDR
- Other 800G Interconnect requirements

Ordering Information

	Part No.	Description
Manufacture PN	EN-OSFP800-2FR4	800 Gb/s 2FR4 OSFP Optical Transceiver with Dual Duplex LC Optical Connector, open top, 2km Reach

Functional Block Diagram

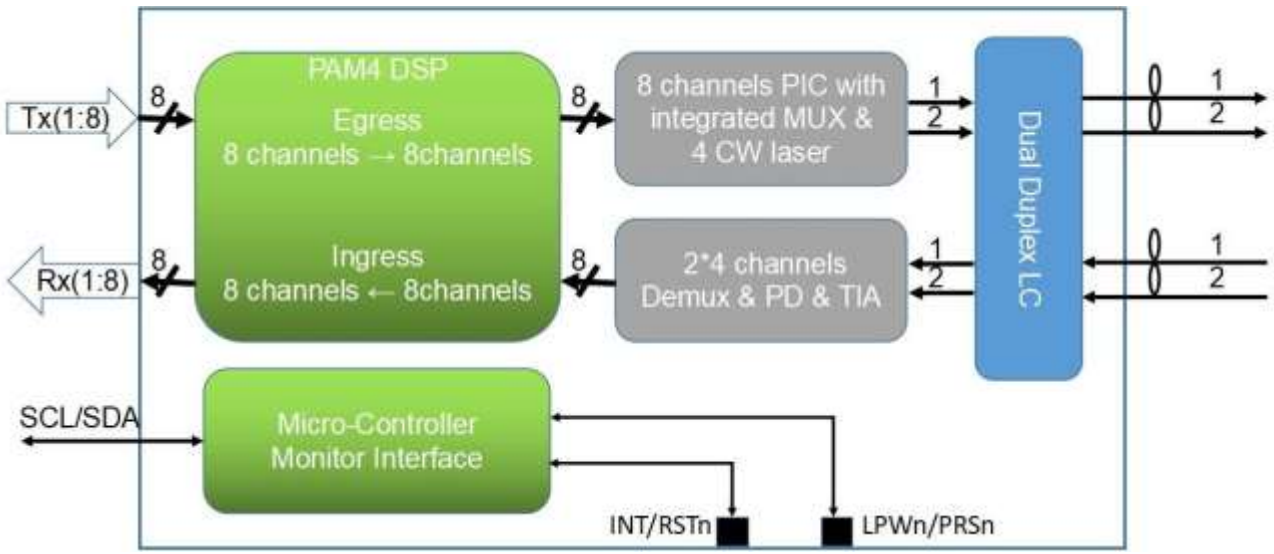

Figure 1 800G OSFP 2FR4 Functional Block Diagram

Pin Assignment

The electrical interface of OSFP module consists of a 60 contacts edge connector as illustrated by the diagram in the figure below, which is defined in Clause 15.1 of OSFP MSA Specification Rev 5.22.

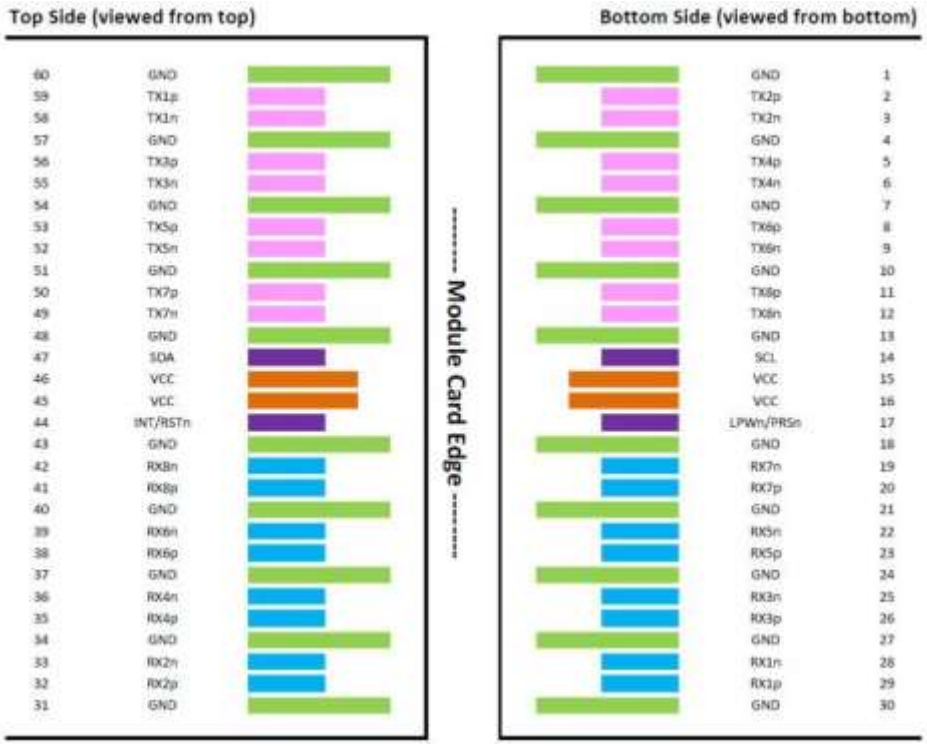

Figure 2 OSFP module pinout

Pin Descriptions

Name	Logic	Direction	Description
TX[8:1]p	CML-I	Input	Transmit differential pairs from host to module.
TX[8:1]n	CML-I	Input	
RX[8:1]p	CML-O	Output	Receive differential pairs from module to host.
RX[8:1]n	CML-O	Output	
SCL	LVCMOS-I/O	Bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	LVCMOS-I/O	Bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	Multi-Level	Bidir	Multi-level signal for low power control from host to module and module presence indication from module to host.
INT/RSTn	Multi-Level	Bidir	Multi-level signal for interrupt request from module to host and reset control from host to module.
VCC	\	Power	3.3V power for module.
GND	\	Ground	Module Ground. Logic and power return path.

Pin List

PIN	Logic	Symbol	Description	Notes
1		GND	Ground	
2	CML-I	Tx2p	Transmitter Data Non-Inverted	
3	CML-I	Tx2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	Tx4p	Transmitter Data Non-Inverted	
6	CML-I	Tx4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	Tx6p	Transmitter Data Non-Inverted	
9	CML-I	Tx6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	Tx8p	Transmitter Data Non-Inverted	
12	CML-I	Tx8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	Open-Drain with pull up resistor on Host
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	See pin description
18		GND	Ground	
19	CML-O	Rx7n	Receiver Data Inverted	

PIN	Logic	Symbol	Description	Notes
20	CML-O	Rx7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	Rx5n	Receiver Data Inverted	
23	CML-O	Rx5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	Rx3n	Receiver Data Inverted	
26	CML-O	Rx3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	Rx1n	Receiver Data Inverted	
29	CML-O	Rx1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	Rx2p	Receiver Data Non-Inverted	
33	CML-O	Rx2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	Rx4p	Receiver Data Non-Inverted	
36	CML-O	Rx4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	Rx6p	Receiver Data Non-Inverted	
39	CML-O	Rx6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	Rx8p	Receiver Data Non-Inverted	
42	CML-O	Rx8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	See pin description
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	Open-Drain with pull up resistor on Host
48		GND	Ground	
49	CML-I	Tx7n	Transmitter Data Inverted	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	Tx5n	Transmitter Data Inverted	
53	CML-I	Tx5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	Tx3n	Transmitter Data Inverted	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	

PIN	Logic	Symbol	Description	Notes
57		GND	Ground	
58	CML-I	Tx1n	Transmitter Data Inverted	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	Ts	-40	+85	℃
Relative Humidity	RH	5	85	%
Power Supply Voltage	VCC	-0.3	+3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature Range	Tc	0	/	70	℃
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Baud Rate(Per channel)	BR	53.125 -100ppm	53.125	53.125 +100ppm	GBd

Optical Characteristics

The following optical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Link power budgets							
Power budget (for max TDECQ)				7.8		dB	
Operating distance				2		km	
Channel insertion loss				4		dB	
Allocation for penalties (for max TDECQ)				3.8		dB	
Transmitter (per Lane)							
Signaling rate per Lane			53.125 -100ppm	53.125	53.125 +100ppm	GBd	
Modulation format				PAM4			
Lane wavelengths		λ_1	1264.5	1271	1277.5	nm	
		λ_2	1284.5	1291	1297.5	nm	
		λ_3	1304.5	1311	1317.5	nm	
		λ_4	1324.5	1331	1337.5	nm	
Side-mode suppression Ratio		SMSR	30			dB	
Average launch power, each lane		P_{AVG}	-3.2		4.4	dBm	1
Outer Optical Modulation Amplitude, each lane	for TDECQ<1.4 dB	OMA_{outer}	-0.2		3.7	dBm	
	for 1.4dB≤TDECQ≤ 3.4dB		- 1.6 + TDECQ		3.7	dBm	
Transmitter and dispersion eye closure for PAM4		TDECQ			3.4	dB	
Transmitter eye closure for PAM4		TECQ			3.4	dB	
| TDECQ– TECQ |					2.5	dB	
Over/under-shoot					22	%	
Transmitter power excursion					1.8	dBm	
Extinction Ratio, each lane		ER	3.5			dB	
Transmitter transition time					17	ps	
Average Launch Power of OFF Transmitter					-16	dBm	
$RIN_{17.1}OMA$					-136	dB/Hz	
Optical Return Loss Tolerance					17.1	dB	
Transmitter reflectance					-26	dB	2

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Receiver (per Lane)							
Signaling rate per Lane			53.125 -100ppm	53.125	53.125 +100ppm	GBd	
Modulation format				PAM4			
Lane wavelengths		λ_1	1264.5	1271	1277.5	nm	
		λ_2	1284.5	1291	1297.5	nm	
		λ_3	1304.5	1311	1317.5	nm	
		λ_4	1324.5	1331	1337.5	nm	
Damage threshold, each lane			5.4			dBm	
Average receive power, each lane			-7.2		4.4	dBm	
Receive power (OMA_{outer}), each lane					3.7	dBm	
Receiver sensitivity (OMA_{outer}), each lane	for TECQ<1.4dB				-4.6	dBm	
	for 1.4dB≤ TECQ≤3.4dB				-6+TECQ	dBm	
Receiver reflectance					-26	dB	
Stressed receiver sensitivity (OMA_{outer})					-2.6	dBm	3
Conditions of stressed receiver sensitivity test							
Stressed eye closure for PAM4 (SECQ), lane under test				3.4		dB	
OMA_{outer} of each aggressor lane				1.4		dBm	

Notes:

1. *Optical output power, each lane (min) is informative and not the principal indicator of signal strength*
2. *Transmitter reflectance is defined looking into the transmitter*
3. *Measured with conformance test signal at TP3 .*

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage		V_{CC}	3.135		3.465	V	
Power Consumption		Pc			16	W	
Module Input							
Differential peak-to-peak voltage tolerance			750			mV	TP1a
Peak-to-peak AC common-mode voltage tolerance	Low-frequency	VCM_{LF}	32			mV	TP1a
	Full-band	VCM_{FB}	80			mV	TP1a
Differential-mode to common-mode return loss		RLcd	See IEEE Std 802.3ck™-2022, 120G.3.3.3			dB	TP1
Effective return loss		ERL	8.5			dB	TP1
Differential termination mismatch					10	%	TP1
Module stressed input tolerance		See IEEE Std 802.3ck™-2022, 120G.3.4.3					TP1a
Single-ended voltage tolerance range			-0.4 to 3.3			V	TP1a
DC common-mode voltage tolerance			-0.35		2.85	V	TP1
Module Output							
Differential peak-to-peak output voltage	short mode				600	mV	TP4
	long mode				845	mV	TP4
Peak-to-peak AC common-mode voltage	Low-frequency	VCM_{LF}			32	mV	TP4
	Full-band	VCM_{FB}			80	mV	TP4
Eye height			15			mV	TP4
Vertical eye closure		VEC			12	dB	TP4
Common-mode to differential-mode return loss		RLdc	See IEEE Std 802.3ck™-2022, 120G.3.1.1			dB	TP4
Effective return loss		ERL	8.5			dB	TP4
Differential termination mismatch					10	%	TP4
Transition time			8.5			ps	TP4
Common Mode Voltage		Vcm	-0.35		2.85	V	TP4
Low Speed Signal							
SCL and SDA		V_{OL}	0		0.4	V	IOL(max)= 3 mA for fast mode, 20 mA for Fast-mode plus
		V_{IL}	-0.3		V_{CC}*0.3	V	
		V_{IH}	V_{CC}*0.7		V_{CC}+0.5	V	

Soft Control, Alarm and Status Timing

Timing specifications for control inputs and alarm/warning and status indicators are described below. Note that alarm and warning flag thresholds are defined in the respective memory map registers.

Parameter	Symbol	Min	Max	Unit	Notes
Time to reach manageability in ModuleLowPwr	tMgmtInit		2000	ms	Time from power on, hot plug, or rising edge of reset until completion of MgmtInit state
Reset Assert Time	t_reset_init	10		µs	Minimum pulse time on Reset signal to initiate a module reset
Interrupt Assert Time	ton_Int		200	ms	Time from onset of condition or occurrence of event until associated unmasked Interrupt asserted
Interrupt De_Assert Time	toff_Int		500	µs	Time from reading (clear on read) last Flag set until Interrupt deasserted, assuming that no conditions nor events causing a Flag setting are present
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1) and Int asserted
Tx Disable Assert Time	ton_txdis		100	ms	Time from Tx Disable bit set (value = 1)until optical output falls below 10% of nominal
Tx Disable De_Assert Time	toff_txdis		400	ms	Time from Tx Disable bit cleared (value = 0) until optical output rises above 90% of nominal
Tx Failure Interrupt Assert Time	ton_Txfail		200	ms	Time from Tx Failure state to Tx Failure Flag raised and Interrupt asserted
Alarm and Warning Flag Assert Time	ton_flag		200	ms	Time from onset of condition or occurrence of event to associated Flag bit raised and Interrupt asserted
Mask Assert Time	ton_mask		100	ms	Time from Mask bit raised while associated Flag bit is set until Interrupt de_Asserted
Mask De_Assert Time	toff_mask		100	ms	Time from Mask bit ceased while associated Flag bit is set until Interrupt asserted
Rx Squelch Assert Time	ton_Rxsq		15	ms	Time from loss of Rx input signal until squelched output condition is reached
Tx Squelch Assert Time	ton_Txsq		400	ms	Time from loss of Tx input signal until squelched output condition is reached
Rx Output Disable Assert Time	ton_rxdis		100	ms	Time from Rx Output Disable bit set (value = 1) until Rx output falls below 10% of nominal
Rx Output Disable De_Assert Time	toff_rxdis		100	ms	Time from Rx Output Disable bit cleared (value = 0) until Rx output rises above 90% of nominal

DDM Accuracy

Parameter	Range	Unit	Accuracy	Calibration
Temperature	-5 to 75	℃	+/-3℃	Internal
Voltage	2.97 to 3.63	V	+/-0.1V	Internal
Tx Bias Current (Each Lane)	20 to 400	mA	10%	Internal
Tx Output Power (Each Lane)	-3.2 to +4.4	dBm	+/-3dB	Internal
Rx Receive Power (Each Lane)	-7.2 to +4.4	dBm	+/-3dB	Internal

Management Interface (I^2C) Timing

		Fast Mode		Fast Mode+			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.50		μs	
Clock Pulse Width High	tHIGH	0.6		0.26		μs	
START Hold Time	tHD.STA	0.6		0.26		μs	
START Setup Time	tSU.STA	0.6		0.26		μs	
Data In Hold Time	tHD.DAT	0		0		μs	
Data In Setup Time	tSU.DAT	0.1		0.1		μs	
Input Rise Time	tR		300		120	ns	
Input Fall Time	tF		300		120	ns	
STOP Setup Time	tSU.STO	0.6		0.26		μs	
STOP Hold Time	tHD.STO	0.6		0.26		μs	
Clock Stretching			500		500	μs	

Memory Map

Refer to OIF-CMIS-05.2 – Common Management Interface Specification (CMIS) Revision 5.2

Regulatory and Compliance

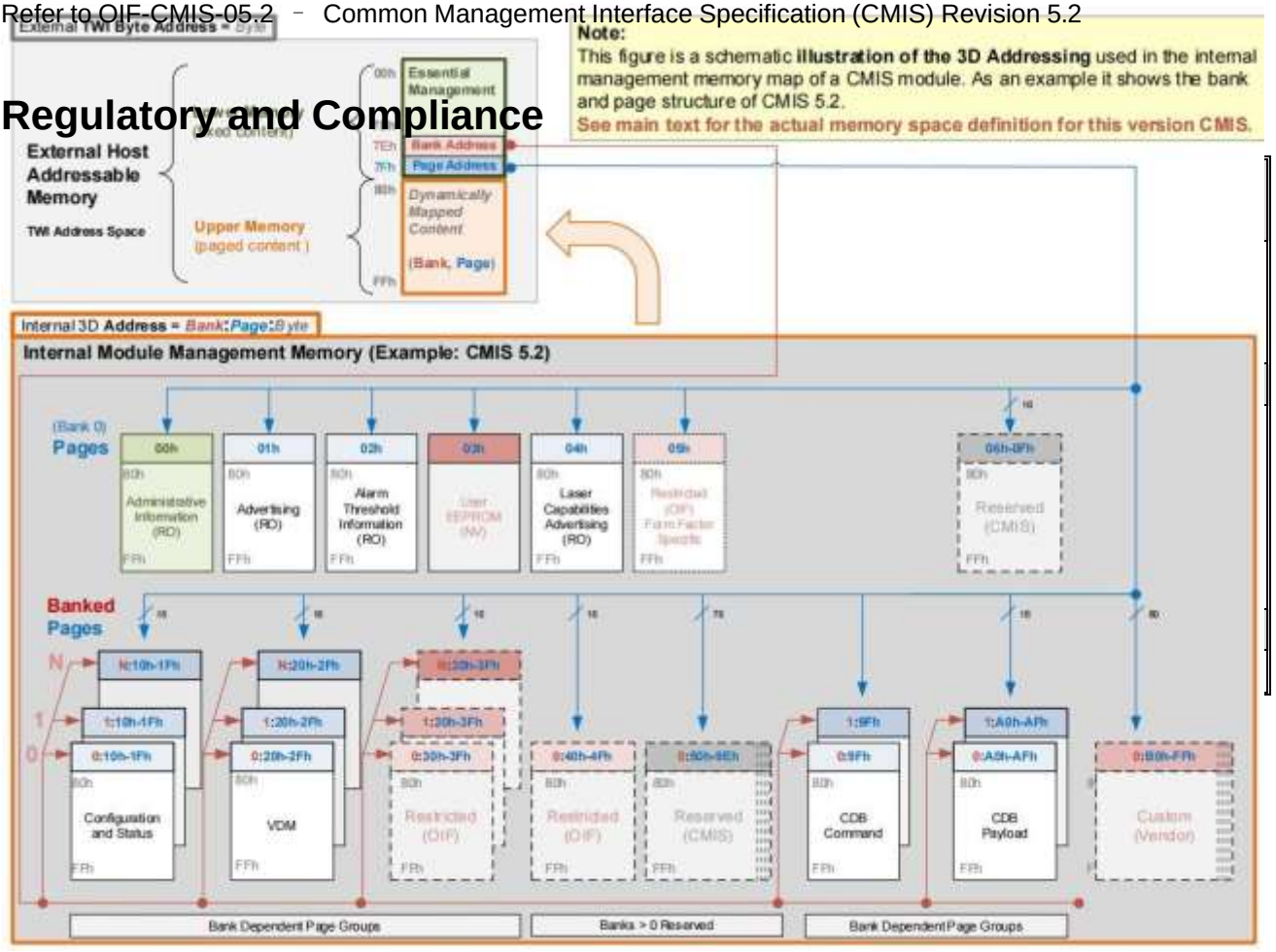

Figure 3 Digital Diagnostic Memory Map

Recommended OSFP Host Board Schematic

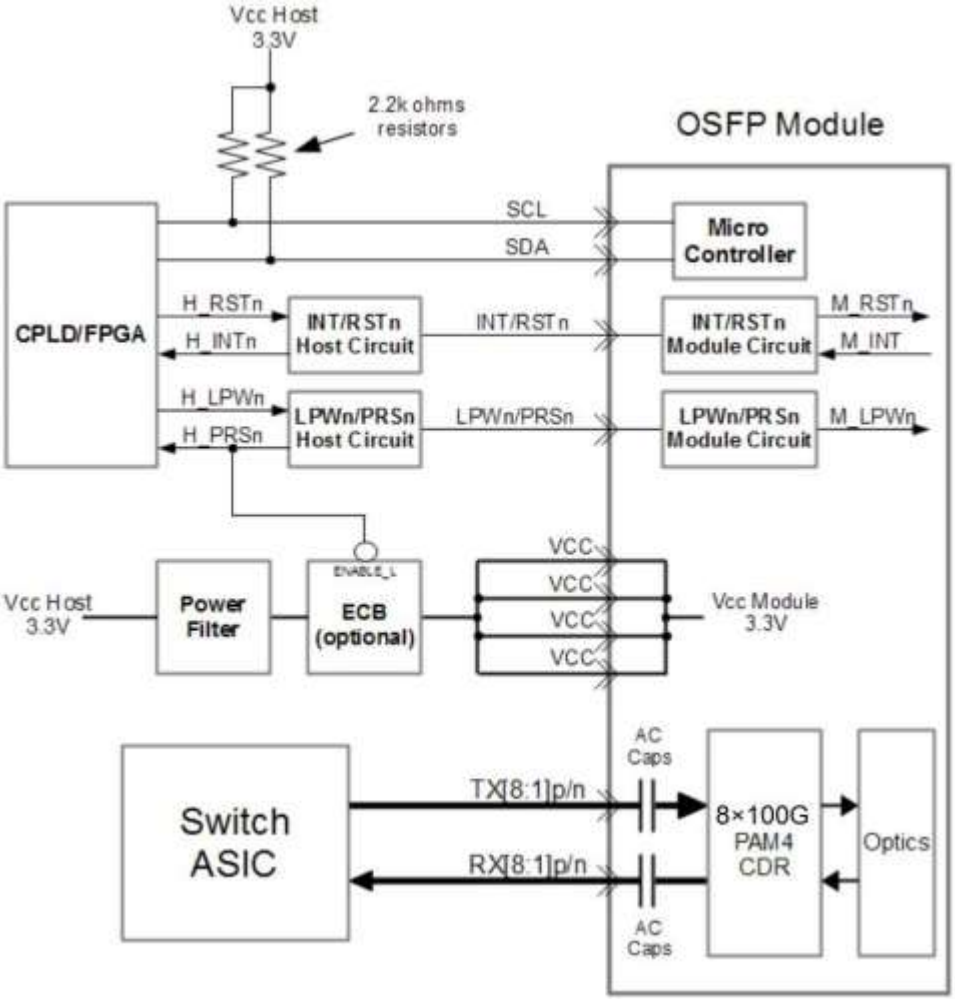

Figure 4 Application Reference Diagram

Host Board Power Supply Filtering

Below is figure that provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

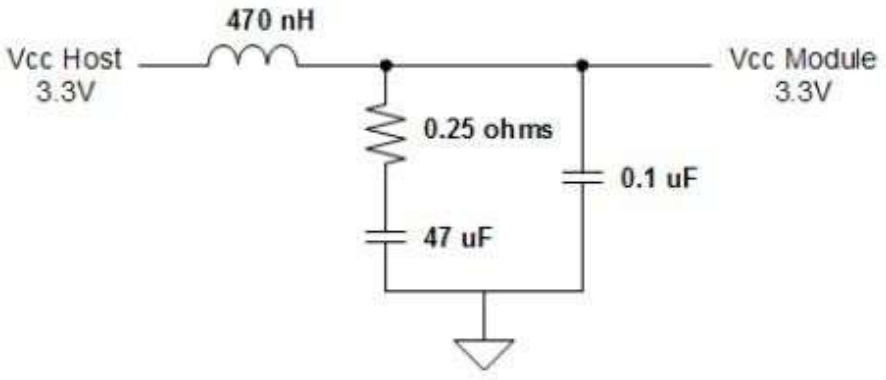

Figure 5 Recommended Power Supply Filter

Regulatory and Compliance

EMC — Immunity	• EN 55035:2017+A11:2020 • IEC EN 61000-4-3 (International)
EMC — Emission	• FCC 47 CFR Part 15, class B • EN 55032:2015+A11:2020+a1:2020
ESD Threshold	• IEC EN 61000-4-2; +/- 8kV contact, +/- 15kV air.
Product Safety	• CB: IEC 62368-1:2018 • TUV Mark: EN IEC 62368-1:2020+A11 • UL Recognized Component: UL 62368-1:2019 R10.21, CSA C22.2 NO. 62368-1:19
Optical Safety	Class 1 laser product • FDA/CDRH • IEC 60825-1:2014 • IEC 60825-2:2021 • EN 60825-1:2014+A11
RoHS	• Complies with RoHS II Directive 2011/65/EU

Mechanical Package Outline

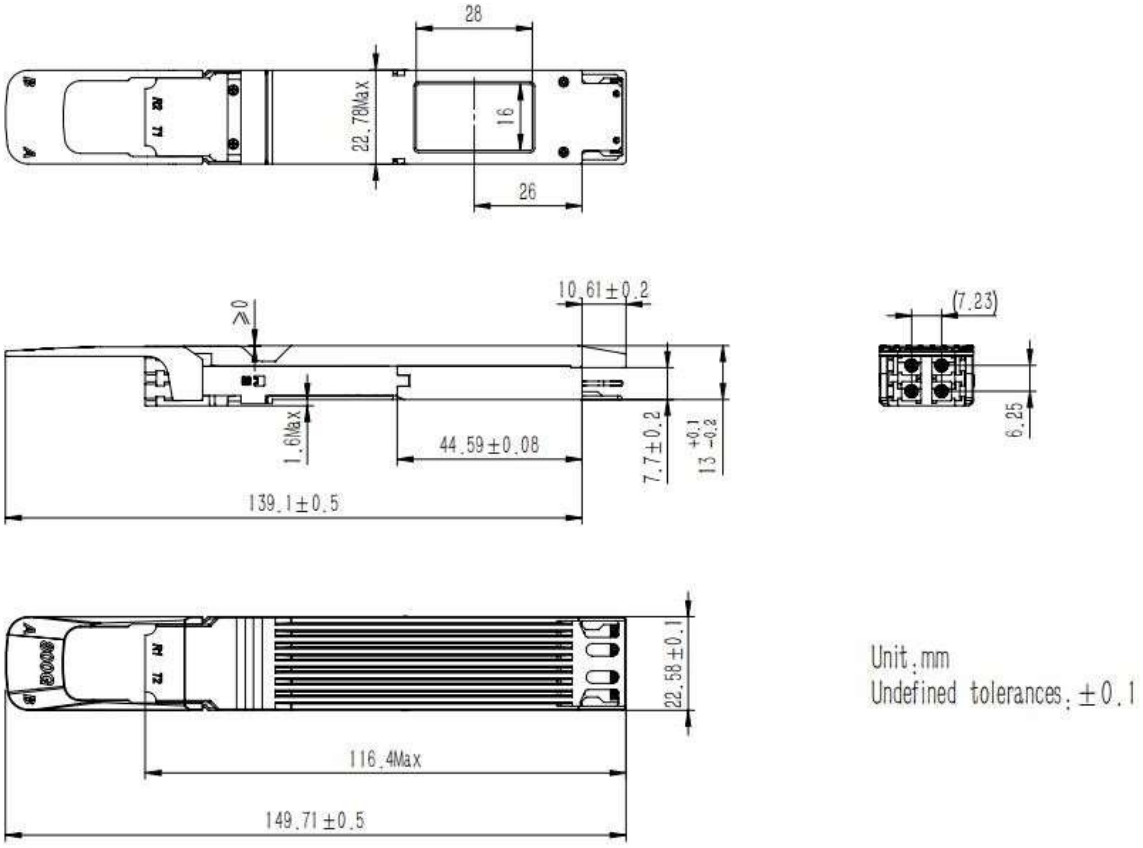

Figure 6 Mechanical Package Outline (All dimensions are in mm)

Optical Interface

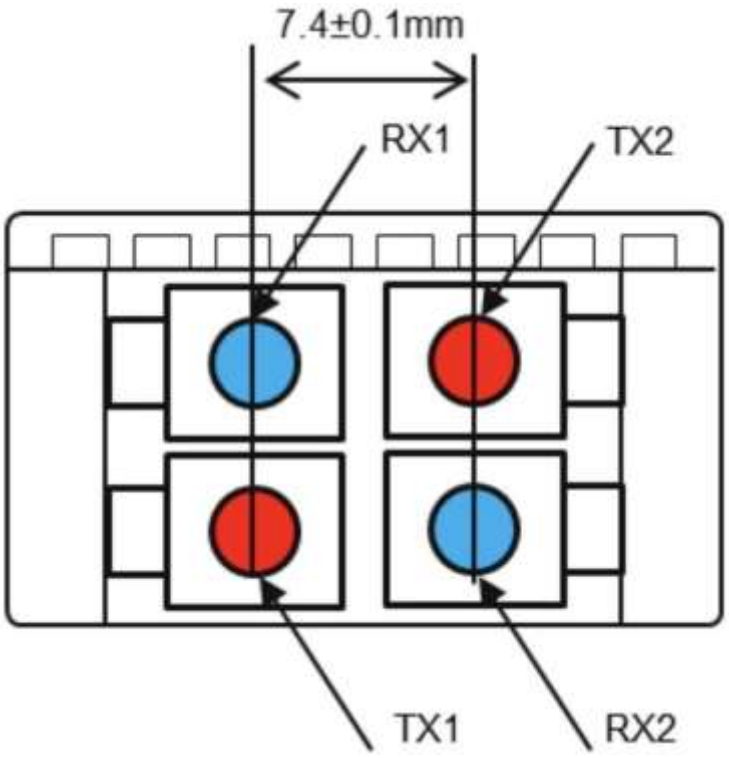

Figure 7 Optical receptacle and channel orientation for Dual LC connector

Force Specification

Measurement	Min	Max	Unit	Notes
OSFP Module Insertion	N/A	40 (55)	N	Module to be inserted into connector and cage with latch mechanism engaged. (55N if the cage has riding heatsink)
OSFP Module Extraction	N/A	30 (45)	N	Module to be removed from connector and cage with latching mechanism disengaged. (45N if the cage has riding heatsink)
OSFP Module Retention in Cage	125	N/A	N	No functional damage to module, connector, or cage with latching mechanism activated. If the module has a pull tab, the pull tab should be able to withstand up to 90N of the pulling under max operating temperature of the module.

Reference Documents

1. *OIF-CMIS-05.2 – Common Management Interface Specification (CMIS) Revision 5.2*
2. *OSFP MSA Specification for OSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE Rev 5.22.*
3. *IEEE Std 802.3ck™–2022*
4. *IEEE Std 802.3-2022™*