

800G OSFP SR8 MPO-16 finned top Datasheet V1.0



The 800G OSFP SR8 Transceiver is designed to transmit and receive serial optical data links up to 106.25 Gb/s data rate (per channel) by PAM4 modulation format over multi-mode fiber. It is a small-form-factor hot pluggable transceiver module integrated with the high performance VCSEL laser and high sensitivity PIN receiver. It is compliant with 800G Ethernet specs and OSFP MSA.

Features

- Up to 106.25Gbps data rate per channel by PAM4 modulation
- 8 duplex channels transmitters and receivers
- MPO-16 APC optical interface
- Single +3.3V power supply
- DDM function implemented
- Hot-pluggable OSFP form factor
- Maximum link length of 100M on OM4 MMF
- Power dissipation: <16W
- International class 1 laser safety certified
- Operating temperature range: 25°C ~ +70°C
- Compliant with ROHS2.0

Applications

- 800GBASE-SR8 Ethernet
- Switch & Router Connections
- Data Centers
- Other 800G/400G Interconnect Requirements.

Standards

- IEEE 802.3db
- IEEE P802.3ck™/D3.0
- OSFP MSA Rev 5.0
- CMIS Rev 5.2

Document History

VER. & STATUS	DATE	DESCRIPTION OF CHANGE	Modifier
1.0	2025-4-18	Initial Release	SYC

Specifications

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter (per Lane)						
Signaling Speed per Lane		GBd		53.125± 100ppm		
Modulation format				PAM4		
Center wavelength		nm	844	850	868	
RMS Spectral Width	RMS	nm			0.6	
Average Launch Power per Lane	TXPx	dBm	-4.6		4	
Outer Optical Modulation Amplitude per Lane	OMA _{outer}	dBm	-2.6		3.5	
Transmitter excursion, each lane	DPx	dB			2.3	
Optical Extinction Ratio	ER	dB	2.5			
Transmitter and dispersion penalty eye closure for PAM4, each lane	TDECQ	dB			4.4	
Transmitter transition time	Tr, Tf	ps			17	
RIN ₁₄ OMA		dB/Hz			-132	
Encircled Flux	FLX	dBm	>86% at 19um			
			<30%at 4.5um			
Optical Return Loss Tolerance	ORL	dB			14	
Average launch power of OFF Transmitter, each lane		dBm			-30	
Receiver(per Lane)						
Signaling Speed per Lane		GBd		53.125± 100ppm		
Modulation format				PAM4		
Center wavelength		nm	844		868	
Damage Threshold	DT	dBm	5			
Average receive Power per Lane	RXPx	dBm	-6.4		4	
Receive power, each lane (OMA _{outer})		dBm			3.5	
Receiver reflectance	R _{fl}	dB			-15	
Receiver sensitivity (OMA _{outer}),		dBm			-4.6	



Stressed receiver sensitivity(OMAouter),each lane	S	dBm			-2	BER=2.4E-4
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Ordering Information

Part No.	Specifications									Application
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reac h	Others	
EN-OSFP800-SR8-M16	OSFP	800G	VCSEL	-4.6~4dBm	PD	< -4.6dBm@ 2.4E-4	25~70°C	100m	RoHS	800GBase SR8

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	°C	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.3	+3.6

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tca	°C	25	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Bit Rate(Per channel)	BR	Gbps		106.25	
Humidity	Rh	%	5		85
Fiber Bend Radius	Rb	cm	6		

Optical Interface

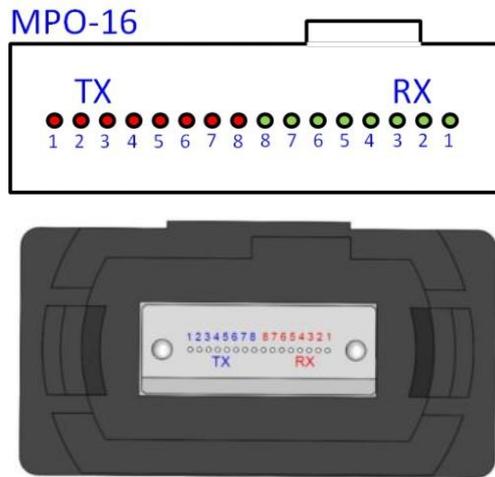


Figure 1. Optical lane sequence

Note: Optical interface is 8° APC MPO-16. Lane sequence is shown in figure 1.

Principle diagram

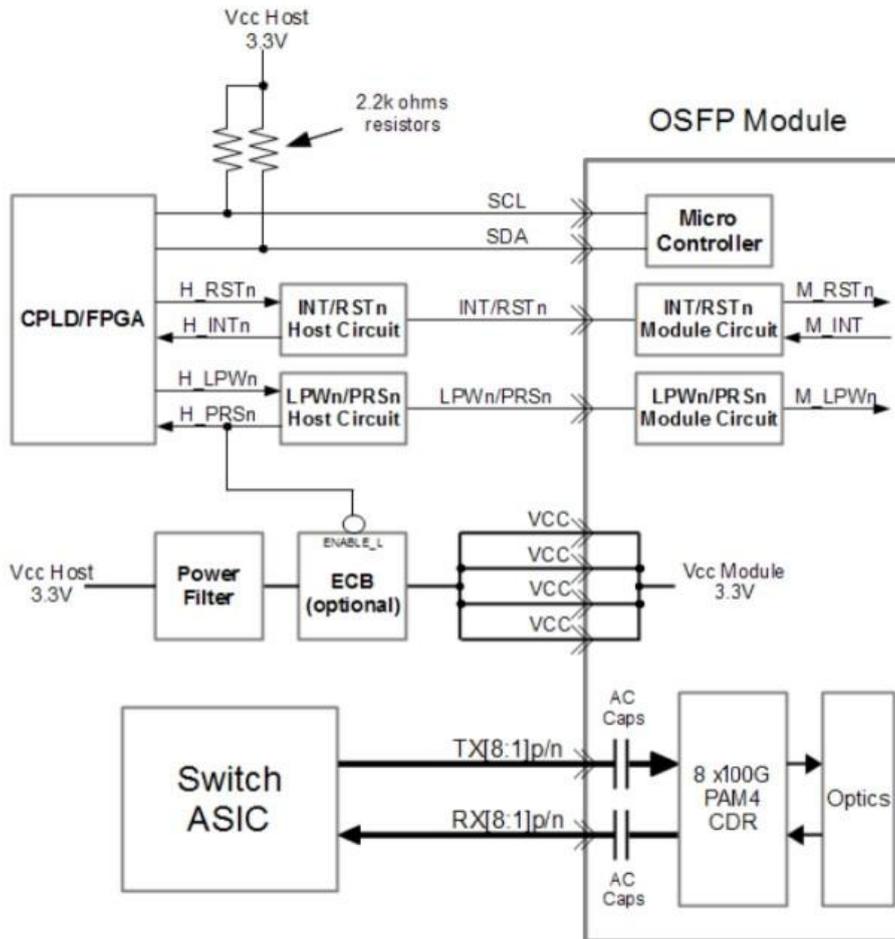


Figure 2. Module Principal Diagram

Electric Ports Definition

Parameter	Min	Typ	Max	Unit	Notes
Supply voltage	3.135		3.465	V	
Signaling rate, each lane	53.125 -100ppm	53.125	53.125 +100ppm	GBd	
Module input characteristics					
Differential peak-to-peak input voltage tolerance	750			mV	TP1a
Peak-to-peak AC common-mode voltage tolerance					TP1a
Low-frequency, $V_{CM_{LF}}$	32			mV	
Full-band, $V_{CM_{FB}}$	80			mV	
Differential-mode to common-mode return loss, RLcd	See IEEE Std 802.3ck™-2022 Equation(120G-2)			dB	TP1
Effective return loss, ERL	8.5			dB	TP1
Differential termination mismatch			10	%	TP1
Module stressed input tolerance	See IEEE Std 802.3ck™-2022 120G.3.4.3				TP1a
Single-ended voltage tolerance	-0.4		3.3	V	TP1a
DC common-mode voltage tolerance	-0.35		2.85	V	TP1
Module output characteristics					
Peak-to-peak AC common-mode voltage					TP4
Low-frequency, $V_{CM_{LF}}$			32	mV	
Full-band, $V_{CM_{FB}}$			80	mV	
Differential peak-to-peak output voltage					TP4
Short mode			600	mV	
Long mode			845	mV	
Eye height	15			mV	TP4
Vertical eye closure, VEC			12	dB	TP4
Common-mode to differential-mode return loss, RLdc	See IEEE Std 802.3ck™-2022 Equation(120G-1)			dB	TP4
Effective return loss, ERL	8.5			dB	TP4



Differential termination mismatch			10	%	TP4
Parameter	Min	Typ	Max	Unit	Notes
Transition time	8.5			ps	TP4
DC common-mode voltage tolerance	-0.35		2.85	V	TP4
IIC communication					
IIC Clock frequency	100		1000	kHz	
Clock stretching			500	μs	
Data In Hold Time	0			μs	
Data In Setup Time	0.1			μs	

Pin Description

Name	Direction	DESCRIPTION
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receive differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host.
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module.
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

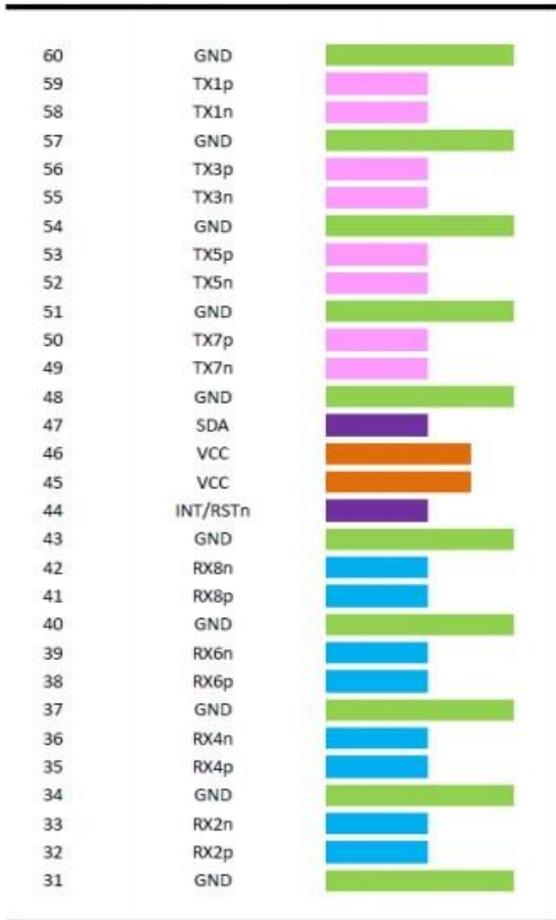
Pin List

PIN	Logic	Symbol	DESCRIPTION	NOTE
1		GND	Ground	
2	CML-I	Tx2p	Transmitter Data Non-Inverted	
3	CML-I	Tx2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	Tx4p	Transmitter Data Non-Inverted	
6	CML-I	Tx4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	Tx6p	Transmitter Data Non-Inverted	
9	CML-I	Tx6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	Tx8p	Transmitter Data Non-Inverted	
12	CML-I	Tx8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVC MOS-I/O	SCL	2-wire Serial interface clock	Open-Drain with pull up resistor on Host
15		VCC	+3.3V Power	
16		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	See pin description

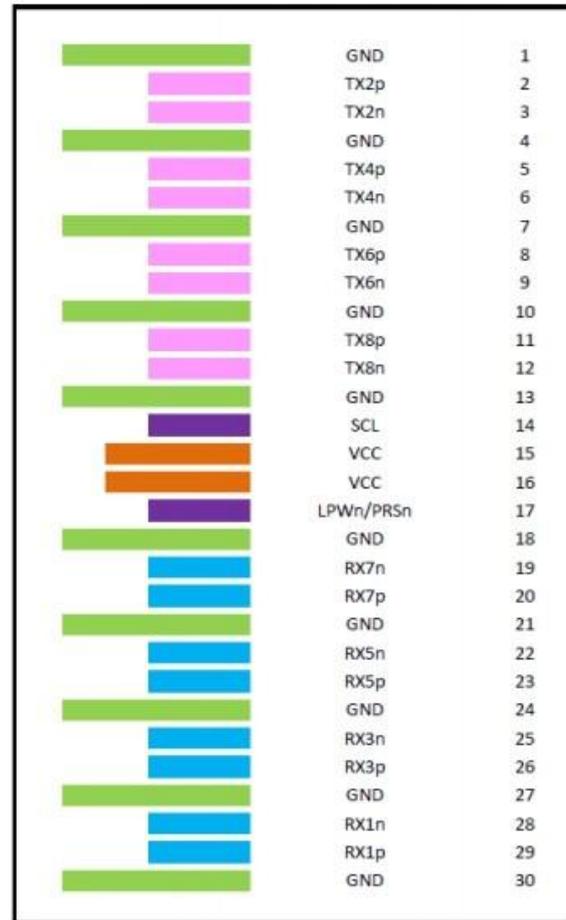
18		GND	Ground	
PIN	Logic	Symbol	DESCRIPTION	NOTE
19	CML-O	Rx7n	Receiver Data Inverted	
20	CML-O	Rx7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	Rx5n	Receiver Data Inverted	
23	CML-O	Rx5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	Rx3n	Receiver Data Inverted	
26	CML-O	Rx3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	Rx1n	Receiver Data Inverted	
29	CML-O	Rx1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	Rx2p	Receiver Data Non-Inverted	
33	CML-O	Rx2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	Rx4p	Receiver Data Non-Inverted	
36	CML-O	Rx4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	Rx6p	Receiver Data Non-Inverted	
39	CML-O	Rx6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	Rx8p	Receiver Data Non-Inverted	
42	CML-O	Rx8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	See pin description
45		VCC	+3.3V Power	
46		VCC	+3.3V Power	
47	LVC MOS-I/O	SDA	2-wire Serial interface data	Open-Drain with pull up resistor on Host
48		GND	Ground	
49	CML-I	Tx7n	Transmitter Data Inverted	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	Tx5n	Transmitter Data Inverted	

53	CML-I	Tx5p	Transmitter Data Non-Inverted	
54		GND	Ground	
PIN	Logic	Symbol	DESCRIPTION	NOTE
55	CML-I	Tx3n	Transmitter Data Inverted	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	
57		GND	Ground	
58	CML-I	Tx1n	Transmitter Data Inverted	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Top Side (viewed from top)



Bottom Side (viewed from bottom)



----- Module Card Edge -----

Figure 3. Electrical Pin-out Details

Module Memory Map

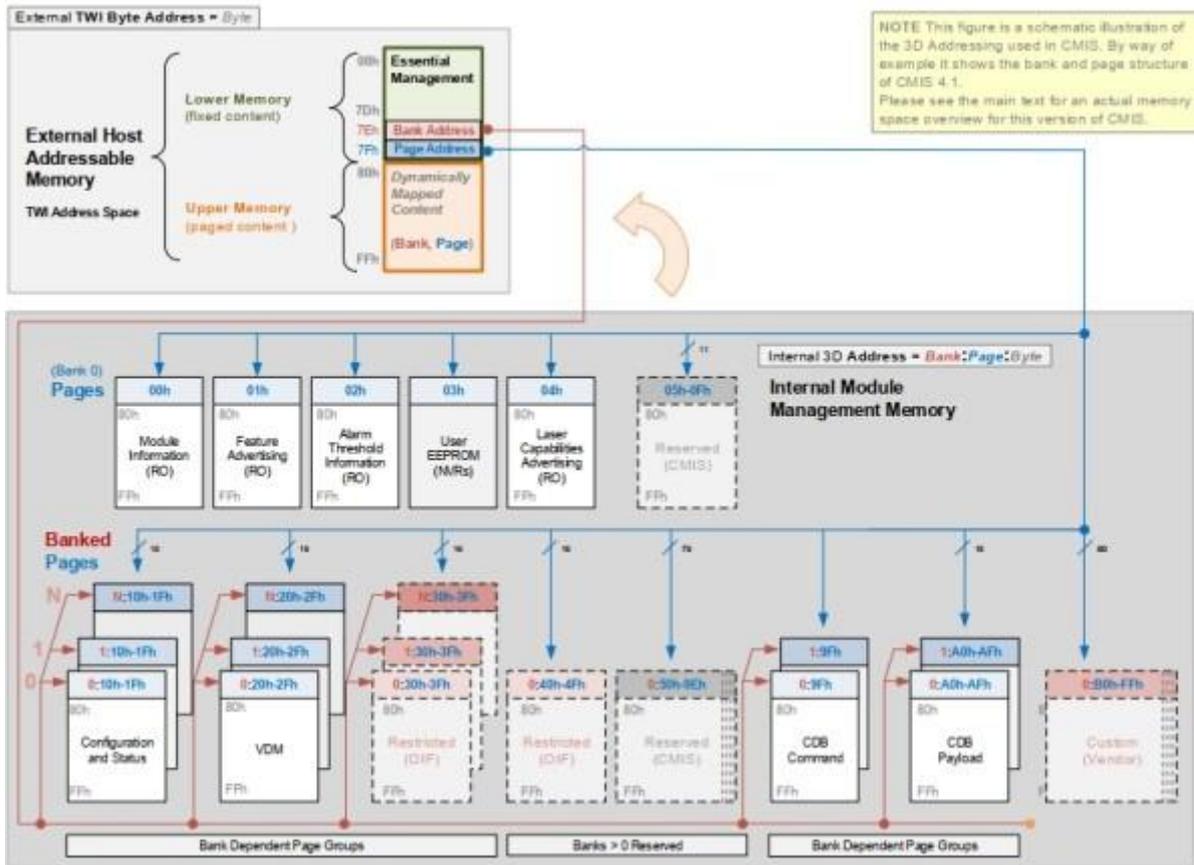


Figure 4 Digital Diagnostic Memory Map

Host Board Power Supply Filtering

Figure 5 provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

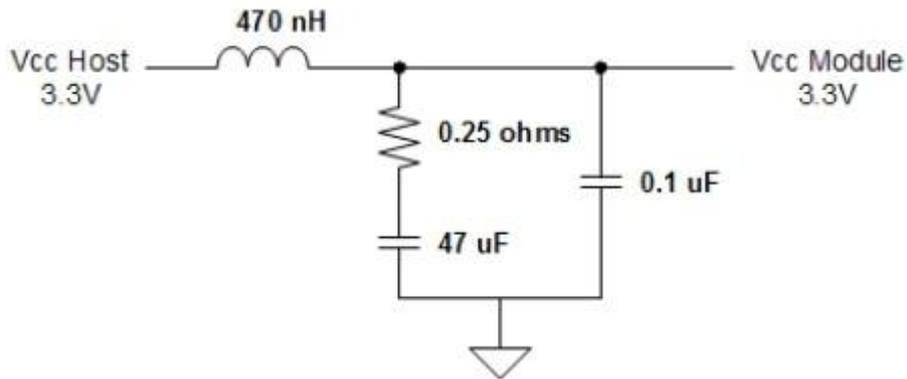


Figure 5 Reference Power Supply Filter for Module Testing

Package Outline

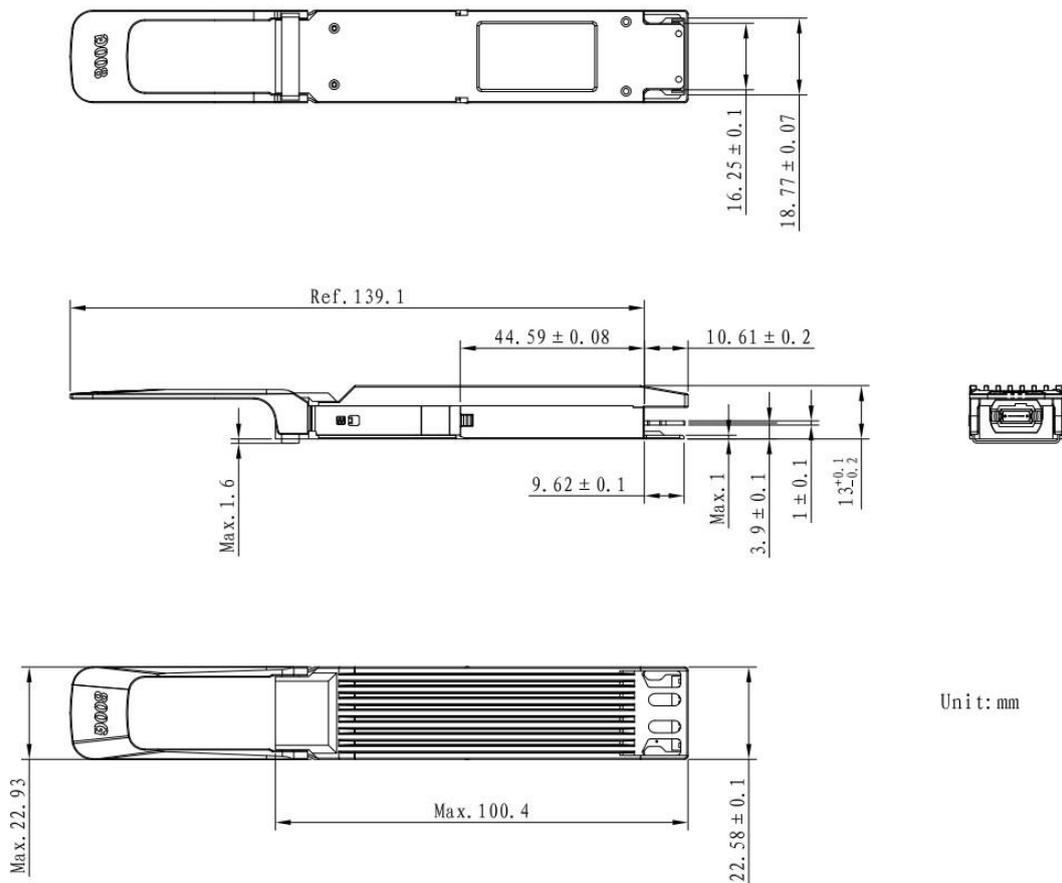


Figure 6 Package Outline